Split-delta background calibration for SAR ADCs

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***Abstract*—This paper introduces a unified performance benchmarking framework which allows to map existing SAR mismatch calibration methods and compare their performance under identical circumstances. Using this framework, an analysis of advantages and disadvantages of popular state-of-the-art methods is presented. Combining the strengths of some of these methods leads to the proposal of a new calibration scheme, coined the split-delta method. This calibration approach is a modification of the split-ADC, yet avoids the more complex architectural modifications required by other split-ADC schemes, while preserving good convergence speed and performance. Finally, the effects that dynamic effects on top of capacitor mismatch and offset have on the converter's SNR are analyzed.**

***Index Terms*—SAR ADC, background calibration, split-ADC, correlation based calibration, ADC high level model**

I. Introduction

The trend in Analog-to-Digital (ADC) converters to go to deep submicron technologies poses new challenges in terms of circuit complexity to counteract the impact of technology scaling. The Successive Approximation Register (SAR) ADC architecture is of great interest in this case, as it is well suited to CMOS scaling and offers a good compromise between sampling rate, power, dynamic range and die area for low-to-medium resolution converters, having found a sweet spot between 8-12 bits [1]. SAR ADC performance is mainly limited by static non-idealities like parasitic capacitances, mismatch in their capacitor array and comparator offset. This can be corrected in the digital domain through calibration, which can be done either offline (foreground) or while the ADC is operating (background) [2]. Dynamic non-linearities like incomplete settling in the capacitive array also affect SAR performance. This can be countered by introducing redundancy in the converter, at the cost of reducing its effective number of bits (ENOB).

Current state of the art background calibration schemes can be broadly divided in three main approaches: a) statistics-based, b) correlation-based, and c) difference-based ADCs. Statistic-based approaches usually require no changes to the ADC architecture, but have been shown to be too slow for practical background calibration [3], [4], and thus will not be further explored in this work. In correlation-based approaches [5]–[7] a pseudo-random noise sequence is injected into the ADC and used to guide the calibration. Lastly, difference-based schemes [8]–[12] execute the same conversion twice, following a slightly different decision path, and exploit the difference in the output obtained by the two conversions to guide the calibration process. Parallel, split and dual-conversion ADC's belong to this category. This paper will introduce a new difference-based calibration scheme enhanced by a controlled offset between the two decisions to boost its robustness and linearity correction capabilities.

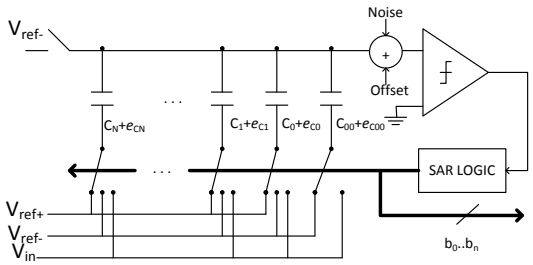


Fig. 1. Main block diagram of a SAR ADC

It is however very difficult to compare the performance of these different schemes in a fair way and assess the best scheme for a particular SAR instantiation. This is due to the fact that all methods have been developed for ADCs with varying characteristics, and in very different validation scenarios, varied number of bits, total capacitance, radix of the converter, implementation technology, application domain, etc. In order to ensure a fair comparison and truly assess the merits of all approaches, a common base model and benchmarking framework is needed. Such framework enables the selection of the best suited calibration method suited for a specific architecture. This paper will present a configurable, unified SAR benchmarking framework in Section II, as well as briefly reference the different algorithms to be tested, and the way they are mapped in the unified model. A modified split-ADC algorithm is introduced in Section III. Section IV presents the results of the unified benchmarking simulations across the different methods to objectively compare the state-of-the-art calibration techniques in the presence of static errors. The effect dynamic errors (settling) have on a SAR converter's performance, and the limitations it imposes on calibration efficiency is also presented. It will be shown that our modified split-ADC technique has a good convergence speed for the LMS correction coefficients, achieves best-in-class post-calibration performance, and yet does not need any complex modification to the ADC implementation. This makes it an excellent trade-off between design complexity and ADC performance.

II. Unified SAR benchmarking framework

A. SAR ADC Unified base model

The basic SAR components are a capacitive DAC (CDAC), a sample and hold switch (S&H), a comparator and the SAR control logic. SAR ADCs are attractive because no linear gain blocks are required; they are power efficient and

amenable to CMOS process scaling. Their main limitations are those of their key building blocks: S&H switch accuracy, capacitor mismatch and parasitic capacitances in the CDAC and comparator noise and offset [1].

The proposed base model consists of different configurable blocks. The block that corresponds to the CDAC can be either differential or single-ended, and can have different architectures besides the classic SAR array, like [13] (A charge recycling CDAC), and is easily expandable to include others. The radix R of the array is also configurable, such that it can be implemented as a binary, sub-binary with a fixed radix or a variable radix array. The configurable digital control automatically matches its switching scheme to the chosen CDAC architecture.

Capacitor mismatch is generated randomly with a normal error probability with zero mean and a given standard deviation σ_u for the LSB unitary capacitor, given as an input to the model. The standard deviation Σ_i of capacitor C_i in the array is:

$$\sigma_i = \sqrt{R^i} * \sigma_u \tag{1}$$

Offset is generated randomly with a configurable standard deviation σ_o.The current modeling assumes an internally synchronous SAR algorithm.

B. Effects of static non-idealities in ADC output

While comparator offset leads to an offset of the entire ADC's transfer curve and can be easily countered digitally, capacitor mismatch can lead to missing codes and missing levels. Errors due to capacitor mismatch occur because the real sizes of the capacitors differ from their ideal value C_i with a mismatch error e_{C_i}. Because of this, the analog bit weights W_i differ from their ideal value W_{ideal} by an error e_{W_i}:

$$W_i = \frac{C_i - e_{C_i}}{C_{00} - e_{C_{00}} + \sum_{k=0}^{k=N} C_k - e_{C_k}} = W_{ideal} - e_{W_i} \tag{2}$$

The quantized input Vin_q is then:

$$Vin_q = \sum_{1}^{N} W_i b_i = \sum_{1}^{N} (W_{ideal} - e_{W_i}) b_i \tag{3}$$

Depending on the implementation of the CDAC, mismatch and parasitic effects can affect these weights differently. E.g. in arrays that employ a bridge capacitor between the MSB and LSB part of the array, each weight corresponding to the LSB part has an error due to the individual mismatch in that capacitor, and all of them have an error that comes from the mismatch in the bridge capacitor. In the end, they can be seen in the same way as eqn. 2, as a weight with error. Each analog value weight has a counterpart $\hat{W}_i$ in the digital domain, which is used to reconstruct the digital output $\hat{X}$ using the raw output bits b_i from the converter. These digital weights are initialized to W_{ideal}, as only the ideal values for Ci are known.

The uncalibrated digital output $\hat{X}$ of the SAR ADC can be then represented as:

$$\hat{X} = \sum_{1}^{N} (\hat{W}_i) b_i = \sum_{1}^{N} (W_{ideal}) b_i = Vin_q + \sum_{1}^{N} e_{W_i} b_i \tag{4}$$

which can be separated into the terms Vin_q (the quantized version of the analog input) and the error term $e_{\hat{X}}$:

$$e_{\hat{X}} = \sum_{1}^{N} e_{W_i} b_i \tag{5}$$

If we add the comparator offset X_{offset} and noise X_{noise}, the final digital output $\hat{X}$ can be seen as:

$$\hat{X} = Vin_q + e_{\hat{X}} + X_{offset} + X_{noise} \tag{6}$$

The idea behind the capacitor calibration of a SAR ADC is to adjust the digital weights $\hat{W}_i$ by estimating and subtracting the weight errors $e_{\hat{W}_i}$ and the value of the comparator offset. These estimates can be obtained by using an LMS algorithm and a reference signal (a known signal in the case of foreground calibration, or a derived signal in the case of background calibration). It is important to note that comparator offset and noise do not affect the linearity of the ADC, while the mismatch in the capacitors and parasitic capacitances do.

C. Overview of SAR calibration methods

The following sections will be briefly overview the major classes of SAR calibration algorithms, and how each of them can easily be mapped onto the common base model for comparative assessment.

1) Correlation-based methods: A pseudo-random noise (PN) sequence is superimposed on the input signal and again digitally subtracted from the reconstructed output. The residue is the final digital output, which is then digitally deconstructed in bits that are individually correlated with the PN sequence to guide the LMS algorithm. If there are no mismatches, or if the calibration process has converged, the PN sequence is completely eliminated and the residue is the correct digital version of the input signal. The speed with which the calibration algorithm converges depends on the amplitude of the PN sequence, and usually millions of samples are required in order to converge [5], [7]. To map this calibration method to the unified model, it is expanded with an additional capacitor to inject an offset during the sampling phase and disconnected during the conversion, so that it does not affect the weight of the rest of the capacitors. To compensate the mismatch of the additional capacitor, an extra LMS coefficient is added to the calibration algorithm. This implementation is based on [7].

2) Difference-based methods: In difference-based methods each sample is converted twice in a way that the difference between the result of the two conversions is nonzero if there are mismatches in the output transfer curve of the ADC, and zero otherwise. As the difference signal in these methods is highly correlated with the error sources, calibration can be achieved with much fewer samples than PN injection

methods [2]. It is important to note that the decision paths of both conversions need to differ to ensure the variables in the LMS algorithm are independent. This paper focuses mainly on split and dual conversion ADCs.

a) Split-ADC: The split ADC approach splits the capacitor array in two almost identical SAR ADCs, each with half the area of the original [9]–[11]. The final output is the average of both conversions. The ADCs are designed such that their outputs differ in case of uncorrected mismatches, but are identical after compensation. The difference ε between them is used to calibrate the ADC weights. The original version of a SAR split-ADC with capacitor calibration is mapped to the common base model of this work, [9]. The difference between the converter branches is used to guide the LMS algorithm. The difference between Split-ADC branches is not enough to guarantee accurate calibration, as it is possible their outputs agree when they both have similar errors. It is necessary then to force both paths to take different decision paths [9], [10]. The implementation in [9] achieves this through its CDAC, where each capacitor in the array is formed by unitary capacitors, which are constantly randomized after each conversion. Because of the randomness induced by this reshuffling, the independence of the branch outputs is guaranteed, so it is possible to calibrate the LMS coefficients even when the input signal is not busy enough, i.e. signals close to DC. An issue with this implementation is that it requires a lot more coefficients (one per unitary capacitor) compared to other methods. Also, the addition of the reconnection matrix for the capacitors is bound to make the actual design of the ADC more complex.

b) Dual-conversion: In dual-conversion ADCs the replication of a parallel ADC is avoided by letting a single ADC convert each sample twice, once with a positive and once a negative offset Δ [12]. The average between them is the output signal, while the error signal ε, the difference between them minus two times Δ should becomes zero if the ADC is calibrated correctly. This error is used to guide the LMS algorithm. The offsets are added using extra capacitors in the sampling DAC, in a similar way as the PN injection explained earlier, hence also leading to additional calibration coefficients in the LMS algorithm. One big disadvantage of this approach is that the conversion time needed by the SAR ADC doubles. As the SAR ADC is already limited in its bandwidth due to its iterative nature, this exacerbates it further, as now twice as many cycles per conversion are needed.

III. Proposed split ADC: Split-delta

This paper introduces an alternative calibration method, the 'split-delta architecture', combining the split ADC idea from [9] and the dual conversion in [12]. This allows having different decision paths in a much simpler scheme, without limiting the conversion speed. A similar process was followed for pipelined-ADC calibration in [14], a difference being that in that approach a PN sequence is used instead of a constant delta. Fig. 2 shows the proposed ADC architecture.

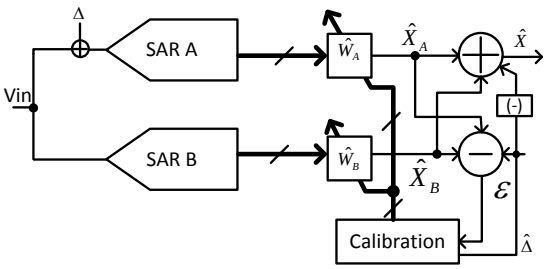


Fig. 2. Split-delta calibration block diagram

In this scheme two conversion outputs are obtained from the same input signal, each coming from a different branch of the split-delta ADC. From here on, they will be referred to as branch *A* and *B*. It is important that the decision paths of these branches differ in order to make the outputs $\hat{X}_A$ and $\hat{X}_B$ independent. This will be guaranteed by adding a controlled offset Δ to one of the branches through a capacitor, just like in the dual-conversion scheme. In the following derivation, Δ is added to branch *A*. The output $\hat{X}$ of the converter is the average of the branch outputs, as seen in eqn.(7). Equations 8 and 9 decompose the branch outputs in its ideal and error components, similar to eqn. 6.

$$\hat{X} = (\hat{X}_A - \hat{\Delta} + \hat{X}_B)/2 \tag{7}$$

$$\hat{X}_A = Vin_q + e_{\hat{X}_A} + \hat{X}_{A_{offset}} + \Delta \tag{8}$$

$$\hat{X}_B = Vin_q + e_{\hat{X}_B} + \hat{X}_{B_{offset}} \tag{9}$$

Because Δ is added through a capacitor, there will be a mismatch $e_{\hat{\Delta}}$ between its analog real value and its digital estimation. The digital value $\hat{\Delta}$ is then:

$$\hat{\Delta} = \Delta + e_{\hat{\Delta}} \tag{10}$$

Just like in previous split ADC schemes, the difference between the branches will direct an LMS algorithm for the bit weight estimation. In this scheme the difference signal ε is obtained by subtracting the output of both branches minus $\hat{\Delta}$. Eqn. 11 shows all the ideal and error components in ε:

$$\begin{aligned} \varepsilon &= \hat{X}_A - \hat{X}_B - \hat{\Delta} \\ &= Vin_q + \Delta + e_{\hat{X}_A} + \hat{X}_{A_{offset}} \\ &- (Vin_q + e_{\hat{X}_B} + \hat{X}_{B_{offset}}) \\ &- (\Delta + e_{\hat{\Delta}}) \end{aligned} \tag{11}$$

It is possible to see the offset in the branches and the mismatch in the Δ capacitor as one single offset error $e_{\hat{\hat{\Delta}}}$, which can be corrected when adjusting the value of $\hat{\Delta}$:

$$e_{\hat{\hat{\Delta}}} = e_{\hat{\Delta}} + \hat{X}_{B_{offset}} - \hat{X}_{A_{offset}} \tag{12}$$

By substituting 12 into 11 and canceling out the ideal terms we obtain: and the digitized offset are calibrated out.

$$\begin{aligned} \varepsilon &= \cancel{Vin_q + \Delta} + e_{\hat{X}_A} - \cancel{Vin_q - \Delta} - e_{\hat{X}_B} - e_{\hat{\hat{\Delta}}} \\ &= \sum_1^n (e_{\hat{W}_{A_i}}) b_{A_i} - \sum_1^n (e_{\hat{W}_{B_i}}) b_{B_i} - e_{\hat{\hat{\Delta}}} \end{aligned} \tag{13}$$

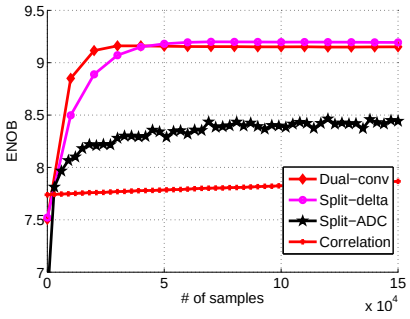


Fig. 3. ENOB convergence of different methods. σ_u = 0.3, N bits = 10 Δ is 32 LSB for split-delta and dual-conversion

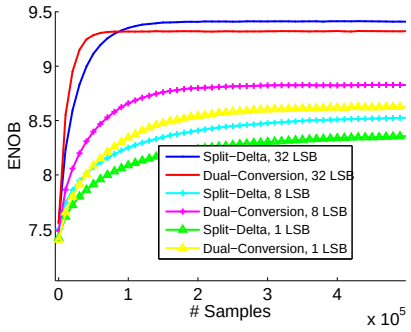


Fig. 4. Effect of delta size in calibration speed and performance, for Dual-conversion and Split-delta

The estimation of e_{X_A},e_{X_B} and $e_{\hat{\Delta}}$ is done through an LMS approach. The value ε is used to guide the LMS convergence. The LMS coefficients are $\hat{W}_A$, $\hat{W}_B$ and $\hat{\Delta}$, and their value at the conversion step $t+1$ is dependent on the value of the bits and the difference signal ε at a given conversion step t:

$$\hat{W}_{A(i,t+1)} = \hat{W}_{A(i,t)} - \mu_w \varepsilon_t b_{Ai} \tag{14}$$

$$\hat{W}_{B(i,t+1)} = \hat{W}_{B(i,t)} - \mu_w \varepsilon_t (-b_{Bi}) \tag{15}$$

$$\hat{\Delta}_{t+1} = \hat{\Delta}_t - \mu_\Delta \varepsilon_t \tag{16}$$

In the simulations presented in this paper the LMS update rate μ_w and μ_Δ are chosen conservatively so the convergence of the algorithm is guaranteed. A value of 2^{-10} and 2^{-12} are used for μ_w and μ_Δ respectively. Higher values would make the algorithm converge faster, at the risk of instability.

IV. Simulation Results and Algorithm Comparison

By configuring the parameters of the unified benchmarking model, it is possible to see the behavior of the algorithms under different conditions.

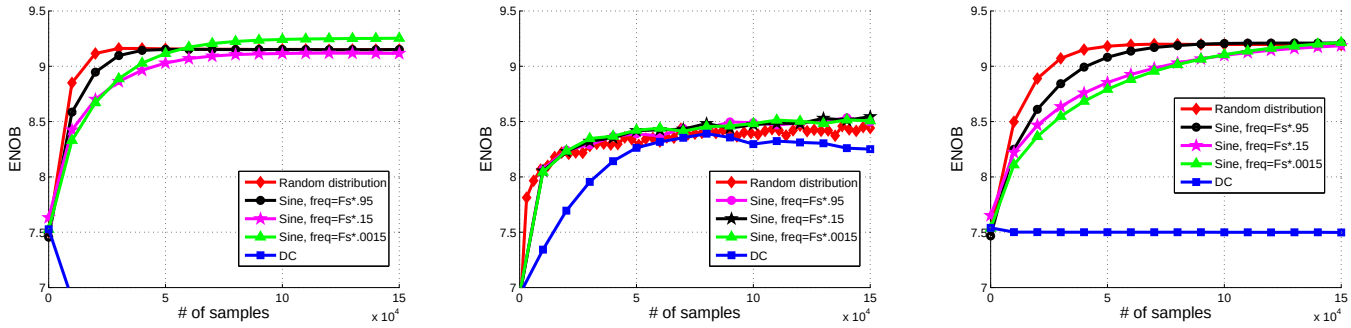
a) Convergence speed: Fig. 3 shows the ENOB evolution curves for the different methods discussed in this work. Each curve is generated by averaging the curves of one hundred Monte Carlo runs, and each point in the curve of one run is generated by calculating the ENOB of the converter every 10k samples. The resolution of the converter is 10 bits, and the capacitor mismatch σ_u is 0.3 (30% of the unitary capacitor value). In order to compare approaches with a split capacitor array vs a single array, the mismatch σ_u of the single array approaches is $\sqrt{2}$ smaller. The input signal is random, with uniform distribution. It can be seen that dual-conversion and split-delta converge fast with good performance. The correlation based approach converges slower due to its weak error signal, requiring about 2e6 samples to converge (not visible in figure). The split-ADC algorithm has a slightly lower performance. This can be explained by Fig. 4; both split-delta and dual-conversion introduce an offset in the ADC branches for calibration, and depending on the size of this offset, the speed and performance of the calibration can improve. This however results in a limitation of the input range, as clipping of one of the branches can severely affect the performance of the algorithm. The limitation itself is not too restrictive (3% reduction in a 10-bit SAR for a 32LSB delta).

b) Input signal effect: Background calibration algorithms are usually dependent on the amplitude distribution of the input signal. Fastest convergence is usually reached with a random signal of uniform distribution, and depending on the algorithm, it might be necessary to turn calibration off if not enough variation in the input samples is present. Fig. 5 shows the effect that different input signals on the tested calibration algorithms. Each curve was generated by averaging the ENOB evolution curve of one hundred Monte Carlo runs, with a σ_u of 0.3 and the converter configured to have 10 bits. The input signals used are a random signal with uniform distribution, 3 tones at 95.1%, 15.1%, 0.151% of the converter's sampling frequency FS, and a DC signal. In general, regardless of the input signal, the original split-ADC converges fastest, followed by dual-conversion and split-delta. Split-delta and dual-conversion are very similar in performance, the difference in convergence speed is due to the fact that split-delta requires twice as many coefficients to calibrate the converter. For all three algorithms it can be seen that random signals converge faster, and as the frequency of the input signal gets closer to DC, the convergence speed drops. The original split-ADC approach on the other hand hardly suffers, as its internal reshuffling scheme ensures varying conversion paths regardless of how busy the input signal is.

c) Tolerance to dynamic errors: The configurable model presented in this work can also simulate capacitor settling errors. In order to add this to the static model presented above, the following equation is used for the output voltage of the CDAC V_{CDAC} at every iteration step n of the SAR search, which is then compared to the sampled signal:

$$V_{CDAC}(n) = \sum_{i=0}^{i=n} W_i b_i e^{-\frac{(n-i+1)T_{cs}}{\tau_i}} \tag{17}$$

Where T_{cs} is the period of a SAR iteration (assuming a synchronous SAR), τ_i is the time constant of each capacitor C_i. At iteration n of the SAR search each capacitor C_i has had $(n-i+1)$ cycles to settle. Fig. 6 shows the tolerance that a redundant capacitor array has for the calibration of static non-idealities in the presence of settling errors. Each point in the curve represents the average of ten Monte Carlo simulations before and after calibration using the split-delta algorithm. In a converter with redundancy it is possible to reduce the



(a) Dual-Conversion (b) Split-ADC (c) Split-delta

Fig. 5. Input signal effect on background calibration for $N = 10$ and $\sigma_u = .3$. Δ is 32 LSB for split-delta and dual-conversion

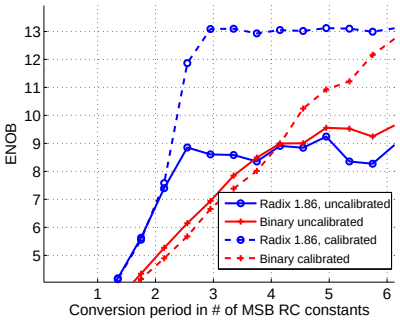


Fig. 6. Dynamic non-idealities and static non-idealities before and after calibration. $N = 14$ and $\sigma_u = .3$

settling time of the capacitors while still being able to reach good performance with calibration. Besides these advantages, redundancy greatly reduces DNL and INL errors. In binary converters even slight capacitor mismatch produces missing codes, while in sub-binary converters redundant codes greatly decrease their occurrence.

V. Conclusion

In this work a unified model to compare different SAR capacitor calibration methods in a fair manner is presented. This common framework allowed to assess the strengths and weaknesses of the different algorithms in the presence of static and dynamic non-idealities and come up with a new approach that combines their advantages. The best results were achieved by the split-delta and the dual-conversion ADCs. The proposed split-delta ADC is a combination of the original split ADC and the dual conversion, and so it has advantages of both, while not requiring to increase the complexity of the ADC architecture. The dual-conversion ADC still has better convergence time and requires half the calibration coefficients and computational complexity of the split-delta, yet this architecture is more constrained in terms of bandwidth. Finally, the original split-ADC implementation is the most robust, as it is independent from the input signal. The effect that incomplete capacitor settling has on calibration was also shown. In conclusion the proposed split-delta SAR ADC allows the execution of background digital calibration with minimal changes to the original ADC array, while showing good convergence speed and digital correction of linearity errors equivalent to more complex methods. An extension of this algorithm for the calibration of non-idealities in pipelined-SAR ADCs is currently being developed.

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